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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/644,801	08/21/2003	Akira Shoji	AIS-0008	7386
23353	7590	08/18/2004	EXAMINER	
RADER FISHMAN & GRAUER PLLC LION BUILDING 1233 20TH STREET N.W., SUITE 501 WASHINGTON, DC 20036			JEANGLAUDE, JEAN BRUNER	
			ART UNIT	PAPER NUMBER
			2819	

DATE MAILED: 08/18/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.

10/644,801

Applicant(s)

SHOJI ET AL.

Examiner

Jean B Jeanglaude

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --
Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 21 August 2003.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-19 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1-19 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 21 August 2003 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
 2. ☐ Certified copies of the priority documents have been received in Application No. _____.
 3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- * See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- 1) ☒ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date 12-22-03.
- 4) ☐ Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____.
- 5) ☐ Notice of Informal Patent Application (PTO-152)
- 6) ☐ Other: _____.

Detailed Action

Abstract

1. Applicant is reminded of the proper language and format for an abstract of the disclosure. The abstract should be in narrative form and generally limited to a single paragraph on a separate sheet within the range of 50 to 150 words. It is important that the abstract not exceed 150 words in length since the space provided for the abstract on the computer tape used by the printer is limited. The form and legal phraseology often used in patent claims, such as "means" and "said," should be avoided. The abstract should describe the disclosure sufficiently to assist readers in deciding whether there is a need for consulting the full patent text for details. The language should be clear and concise and should not repeat information given in the title. It should avoid using phrases which can be implied, such as, "The disclosure concerns," "The disclosure defined by this invention," "The disclosure describes," etc.
2. The abstract should be in narrative form and generally limited to a single paragraph on a separate sheet within the range of 50 to 150 words.

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

4. Claims 1 – 7 are rejected under 35 U.S.C. 102(b) as being anticipated by Cukauskas et al. (US patent number H873).

5. Regarding claims 1, 3, Cukauskas et al. discloses a method (fig. 1) for forming a Josephson junction (abstract) , comprising the steps of forming a two-layer film (the two-layer film are the first passivation layer and the second passivation layer that a deposited on the barrier layer) having an amorphous MgO layer and a high orientation MgO layer on a Si substrate (abstract; col 1, lines 24 – 30) and laminating a NbN film or an NbCN film on the two-layer (fig. 1; abstract; col 1, lines 24 – 30; col 2, line 20).
6. Regarding claim 2, Cukauskas et al. discloses a method (fig. 1; abstract) wherein the NbN film or the NbCN film is used as an electrode (abstract; col 3, lines 7 – 14).
7. Regarding claim 4, Cukauskas et al. discloses a Josephson junction comprises a Si substrate (10) ; a two layer film (14, 18) comprising an amorphous MgO layer and a high orientation MgO layer on the Si substrate (abstract; col 1, lines 24 – 30); and a NbN film or a NbCN film laminated on the two layer film (abstract).
8. Regarding claim 5, Cukauskas et al. discloses a Josephson junction wherein the NbN film or NbCN film is used as an electrode (abstract; col 3, lines 7 – 14).
9. Regarding claim 6, Cukauskas et al. discloses a Joseph junction array (the arrays are not shown) comprising at least one Josephson junction (the junction is not shown) comprises a Si substrate (10) ; a two layer film (14, 18) comprising an amorphous MgO layer and a high orientation MgO layer on the Si substrate (abstract; col 1, lines 24 – 30); and a NbN film or a NbCN film laminated on the two layer film (abstract).
10. Regarding claim 7, Cukauskas et al. discloses a Josephson junction array wherein the NbN film or NbCN film is used as an electrode (abstract; col 3, lines 7 – 14).

Claim Rejections - 35 USC § 103

11. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

12. Claims 8, 9 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hamilton et al. (US Patent Number 5,565,866) in view of Cukauskas et al. (H873).

13. Regarding claims 8, 9, Hamilton et al. discloses a digital to analog converter (fig. 9) comprising a Josephson junction arrays (110 – 113) comprising Josephson junctions (fig. 9; the junction are shown in fig. 9 in the junction arrays). Hamilton et al. does not specifically disclose a Josephson junction wherein at least one of the Josephson junctions comprises a Si substrate, a two layer film comprising an amorphous MgO layer and a high orientation MgO layer on the Si substrate and a NbN film or a NbCN film laminated on the two layer film and a Josephson junction array wherein the NbN film or NbCN film is used as an electrode. However, Cukauskas et al., in a related art, discloses a Joseph junction array (the arrays are not shown) comprising at least one Josephson junction (the junction is not shown) comprises a Si substrate (10) ; a two layer film (14, 18) comprising an amorphous MgO layer and a high orientation MgO layer on the Si substrate (abstract; col 1, lines 24 – 30); and a NbN film or a NbCN film laminated on the two layer film (abstract; col 2, line 20). Also, Cukauskas et al. discloses a Josephson junction array wherein the NbN film or NbCN film is used as an electrode (abstract; col 3, lines 7 – 14). Therefore, it would have been obvious to one of

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ordinary skill in the art at the time the invention was made to couple Cukauskas et al's system in Hamilton et al.'s system in order to provide a strip line or transmission line device in which subsequent layers can be deposited at elevated temperatures without serious degradation to the base electrode/barrier interface (col 2, lines 5 – 22).

14. Claims 10 - 19 are rejected under 35 U.S.C. 103(a) as being unpatentable over Przybysz et al. (US patent Number 5,798,722) in view of Cukauskas et al. (US Patent Number H873).

15. Regarding claims 10 - 13, Przybysz et al. discloses a Josephson voltage generating (standard) apparatus (figs. 1, 4) comprising a digital to analog converter (10, figs. 1, 4) comprising junction arrays (note the JJ arrays in 10) for programmable converter using Josephson junctions (10). Przybysz et al. does not specifically disclose a Josephson voltage generating (standard) apparatus wherein at least one of the Josephson junctions comprises a Si substrate, a two layer film comprising an amorphous MgO layer and a high orientation MgO layer on the Si substrate and a NbN film or a NbCN film laminated on the two layer film and a Josephson junction array wherein the NbN film or NbCN film is used as an electrode. However, Cukauskas et al., in a related art, discloses a Joseph junction array (the arrays are not shown) comprising at least one Josephson junction (the junction is not shown) comprises a Si substrate (10) ; a two layer film (14, 18) comprising an amorphous MgO layer and a high orientation MgO layer on the Si substrate (abstract; col 1, lines 24 – 30); and a NbN film or a NbCN film laminated on the two layer film (abstract; col 2, line 20). Also, Cukauskas et al. discloses a Josephson junction array wherein the NbN film or NbCN

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film is used as an electrode (abstract; col 3, lines 7 – 14). Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to couple Cukauskas et al.'s system in Hamilton et al.'s system in order to provide a strip line or transmission line device in which subsequent layers can be deposited at elevated temperatures without serious degradation to the base electrode/barrier interface (col 2, lines 5 – 22).

16. Regarding claims 14 - 19, it is noted in figs 1 – 6 of Przybysz et al. a superconducting sub-millimeter wave oscillator (a superconducting quantum interference device)(a superconductivity digital integrated circuit) in which Josephson junctions are used. Przybysz et al.'s system does not specifically described the Josephson junction that comprises a Si substrate, a two layer film comprising an amorphous MgO layer and a high orientation MgO layer on the Si substrate and a NbN film or a NbCN film laminated on the two layer film and a superconducting sub-millimeter wave oscillator 9 superconducting quantum interference device) wherein the NbN film or NbCN film is used as an electrode. However, Cukauskas et al., in a related art, discloses a Joseph junction array (the arrays are not shown) comprising at least one Josephson junction (the junction is not shown) comprises a Si substrate (10) ; a two layer film (14, 18) comprising an amorphous MgO layer and a high orientation MgO layer on the Si substrate (abstract; col 1, lines 24 – 30); and a NbN film or a NbCN film laminated on the two layer film (abstract; col 2, line 20). Also, Cukauskas et al. discloses a Josephson junction array (a superconducting quantum interference device)(a superconductivity digital integrated circuit) wherein the NbN film or NbCN film is used

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as an electrode (abstract; col 3, lines 7 – 14). Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to couple Cukauskas et al's system in Hamilton et al.'s system in order to provide a strip line or transmission line device in which subsequent layers can be deposited at elevated temperatures without serious degradation to the base electrode/barrier interface (col 2, lines 5 – 22).

Conclusion

17. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

18. Kroger (US patent Number 4,220,959) discloses a Josephson tunnel Junction with polycrystalline silicon, germanium or silicon-germanium alloy tunneling barrier.

19. Shiraishi et al. (US patent Number 5,229,361) discloses a method for forming Josephson junction devices by radiation.

20. Mueller (US patent Number 5,656,575) discloses a method and apparatus for fabricating weak link junctions on vicinally cut substrates.

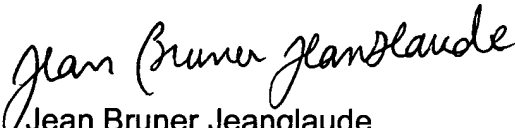
21. Yamamori et al. (US Patent Number 10/441,179 ; US PGPub 2003/0218164) discloses a Josephson Junction.

22. Shoji (JP 2004079882A) discloses a creation method and apparatus of Josephson Junction.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jean B Jeanglaude whose telephone number is 571-272-1804. The examiner can normally be reached on Monday - Friday 7:30 A. M. - 5:00 P.M..

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Michael Tokar can be reached on 571-272-1812. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).


Jean Bruner Jeanglaude
Primary examiner
August 12, 2004